

CLAIMS

1. A distributed architecture system including multiple electronic modules that communicate with each other over a communication bus, including at least one electronic module that transmits messages over said communication bus by modulation of a bus current while receiving messages over said communication bus by de-modulation of a received bus voltage, the improvement comprising:

compensation circuitry responsive to the modulation of the bus current by said at least one electronic module for increasing said received bus voltage by an amount that counteracts decreases in said received bus voltage due to said modulation of bus current.

2. The improvement of Claim 1, wherein:

said bus voltage is received by a receiver circuit of said at least one electronic module; and

- said compensation circuitry includes a compensation resistor coupled between said bus and said receiver circuit, and a current mirror circuit for supplying current to said compensation resistor in proportion to a modulation current drawn from said communication bus by the modulation of said bus current.

3. The improvement of Claim 2, wherein said compensation circuitry further includes:

a charge pump coupled to said communication bus for developing an elevated voltage source for said current mirror circuit

4. The improvement of Claim 2, wherein:

said at least one electronic module is coupled to said communication bus via an input resistance; and

- said compensation resistor has a resistance determined in relation to said input resistance so that the current supplied to said compensation resistor creates a

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5 input resistance so that the current supplied to said compensation resistor creates a
voltage across said compensation resistor that matches a voltage across said input
resistance due to the modulation of said bus current.

5. The improvement of Claim 4, wherein:

said current mirror circuit supplies current to said compensation resistor
based on a predetermined fraction JAR of said modulation current; and

said compensation resistor has a resistance determined according to R_t/JAR ,
5 where R_t is said input resistance.

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